Product Specification

10Gb/s 1550nm Ethernet X2 Transceiver

☑ Features:

- Hot Z-pluggable
- XAUI Electrical Interface: 4lanse@3.125Gbit/s
- Below 4W power dissipation
- SC-Duplex Optical Receptacle
- Digital Diagnostic Monitor Interface
- Very low EMI and excellent ESD protection
- Uncooled 1550nm DFB laser and PIN ROSA
- Up to 40KM for single mode fiber
- Operating temperature range -40°C to 85°C

☑ Applications:

- 10G BASE-ER/EW Ethernet
- SONET OC-192/SDH STM-64 line card
- Other optical links

☑ Standard:

- X2 MSA compliant
- IEEE802.3ae-2002 compliant
- ITU-T G.959 and G.691 compliant
- GR-253-CORE compliant
- RoHS compliant

☑ Description:

WT 's 10GbE X2 transceiver module WT-X2-ER is a hot pluggable in the Z-direction module that is usable in typical router line card applications, Storage, IP network and LAN and compliant to X2 MSA.

The WT-X2-ER is a fully integrated 10.3Gbit/s optical transceiver module that consists of a 10.3Gbit/s optical transmitter and receiver. This version of transceiver line uses a 1550nm EA-DFB Laser Diode to achieve 40km over standard multi mode fiber as specified by 10GBASE-ER in the IEEE 802.3ae standard.

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☑ Pin Definitions:

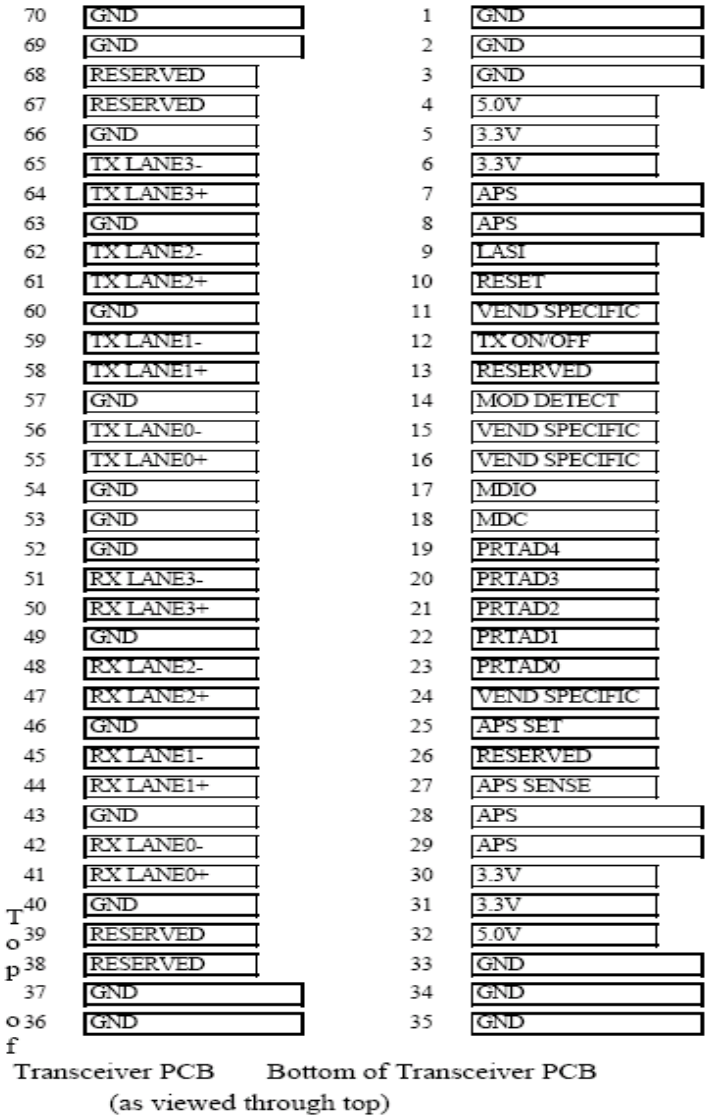
Pin #	Symbol	I/O	Logic	Description	Notes
1	GND	I	Supply	Electrical ground	
2	GND	I	Supply	Electrical ground	
3	GND	I	Supply	Electrical ground	
4	5.0 V	I	Supply	Power	
5	3.3 V	I	Supply	Power	
6	3.3 V	I	Supply	Power	
7	APS	I	Supply	Adaptive Power Supply	
8	APS	I	Supply	Adaptive Power Supply	
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.	
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	
13	RESERVED	-	-	Reserved	
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.	
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	

☑ Pin Definitions:

Pin #	Symbol	I/O	Logic	Description	Notes
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
17	MDIO	I/O	Open Drain	Management Data IO	
18	MDC	I	1.2V CMOS	Management Data Clock	
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)	
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
25	APS SET	O	-	Feedback output for APS	
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.	
27	APS SENSE	O	Analog	APS Sense Connection	
28	APS	I	Supply	Adaptive Power Supply	
29	APS	I	Supply	Adaptive Power Supply	
30	3.3 V	I	Supply	Power	
31	3.3 V	I	Supply	Power	
32	5.0 V	I	Supply	Power	
33	GND	I	Supply	Electrical Ground	
34	GND	I	Supply	Electrical Ground	
35	GND	I	Supply	Electrical Ground	

☑ Pin Definitions:

Pin #	Symbol	I/O	Logic	Description	Notes
36	GND	I	Supply	Electrical Ground	
37	GND	I	Supply	Electrical Ground	
38	RESERVED	-	-	Reserved	
39	RESERVED	-	-	Reserved	
40	GND	I	Supply	Electrical Ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-	
43	GND	I	Supply	Electrical Ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-	
46	GND	I	Supply	Electrical Ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-	
49	GND	I	Supply	Electrical Ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-	
52	GND	I	Supply	Electrical Ground	
53	GND	I	Supply	Electrical Ground	
54	GND	I	Supply	Electrical Ground	
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-	
57	GND	I	Supply	Electrical Ground	
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-	
60	GND	I	Supply	Electrical Ground	
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-	
63	GND	I	Supply	Electrical Ground	
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+	
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-	
66	GND	I	Supply	Electrical Ground	
67	RESERVED	-	-	Reserved	
68	RESERVED	-	-	Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	



☑ Absolute Maximum

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-40	85	°C
Case Temperature	Tc	0	70	°C
Power Supply Voltage	VCC3	0	4.0	V
	Vcc5	0	5.5	V
	Vccaps	0	1.5	V
Operating Relative Humidity	RH		85	%

☑ Electrical Characteristics:

Transmitter(-40~85℃@9.953Gb/s~11.1Gb/s)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
Operating Date Rate			10.3125		Gb/s	
Ave. Output Power	Po			2	dBm	1
Output Centre Wavelength	λ	1530		1565	nm	
Disable Power	Poff			-30	dBm	
Extinction Ratio	ER	3			dB	1
Sidemode Supression Ratio		30			dB	
Rise/Fall Time (20%~80%)	Tr/Tf			45	ps	
OMA		1.7			dBm	1
Signal Speed Variation from nominal		-100		100	ppm	

Receiver(-40~85℃@9.953Gb/s~11.1Gb/s)						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Date Rate			10.312		Gb/s	
Overload	Po	0.5			dBm	
Input Centre Wavelength	λ	1270		1600	nm	
Receiver Sensitivity	Pmin			-16	dBm	1
Stressed Sensitivity in OMA				-11.3	dBm	2
LOS Assert	LosA	-30			dBm	
LOS De-assert	LosD			-18	dBm	
LOS Hysteresis		0.5		4	dB	
Optical Return Loss		14			dB	
Jitter Tolerance			GR-253-CORE/ITU-T G.783			1

Note : 1. Measured at 9.95328Gb/s,Framed PRBS2^31-1,NRZ
2. Measured at 10.3125Gb/s,Non-framed PRBS2^31-1,NRZ

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☑ MDIO Operation:

Frame	Management frame fields							IDLE
	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS/DATA	
Address	1...1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read.inc	1...1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

PRE = Preamble, Which consists of 32bit '1's
ST = Start of Frame indicated by 00 pattern
OP = Access Type
- '00' for Address
- '01' for Write
- '11' for Read
- '10' for Post Read Incremented Address

TA = Turnaround: Z0 for Read, and '10' for Write
PRTAD =Physical Address(hardwired)
DEVAD = Device Type
- '00000' for Reserved
- '00001' for PMA/PMD or User-defined Register(including NVR memory)
- '00010' for WIS(Not implemented)
- '00011' for PCS or X2 Register(including NVR memory)
- '00100' for PHY XS or X2 Register(including NVR memory)
- '00101' for DTE XS(Not implemented)

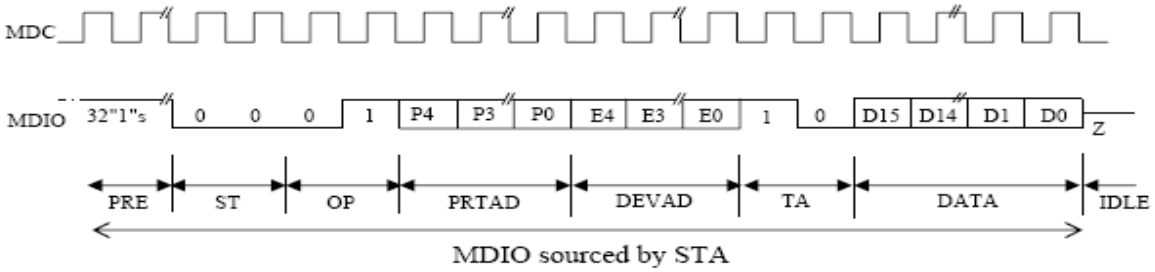

Figure 21 MDIO/MDC Timing Diagram during the Write/Address Operation

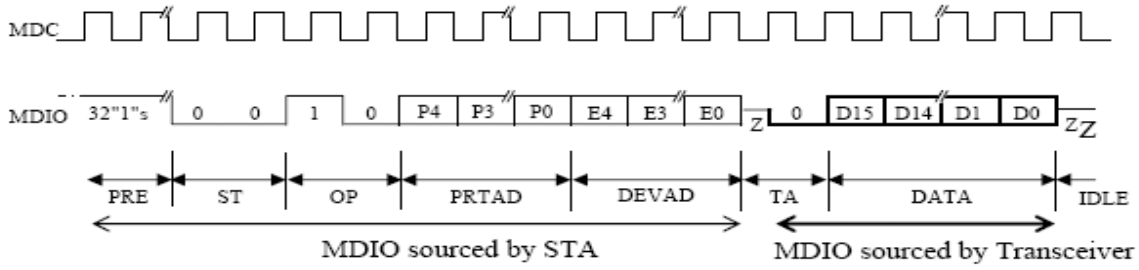

Figure 22 MDIO/MDC Timing Diagram during the Read/Read inc Operation

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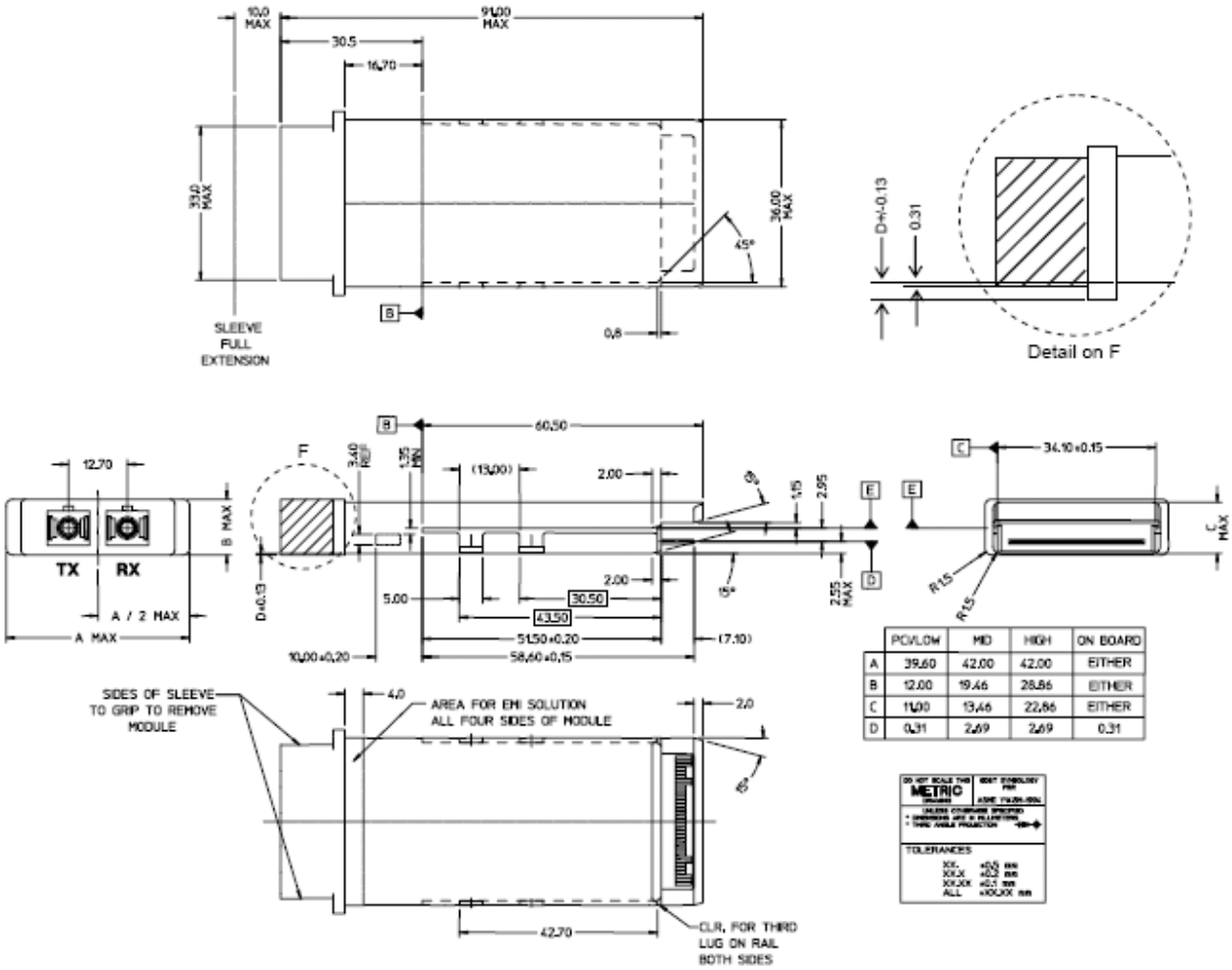
☑ Package Dimensions:



	POWLOW	MID	HIGH	ON BOARD
A	39.60	42.00	42.00	EITHER
B	12.00	19.46	28.86	EITHER
C	11.00	13.46	22.86	EITHER
D	0.31	2.69	2.69	0.31

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